PCIe-7360

100 MHz 32-CH High-Speed Digital I/O Card

PCI EXPRESS®

Introduction

ADLINK's PCIe-7360 is a high-speed digital I/O board with 32-CH bi-directional parallel I/O, with data rates up to 400 MB/s are available through the x4 PCI Express® interface, and clock rates up to 100 MHz internal or 200 MHz external, ideally suiting high speed and large scale digital data acquisition or exchange applications, such as digital image capture, video playback and IC testing.

I/O Port Configuration & Level Shifting

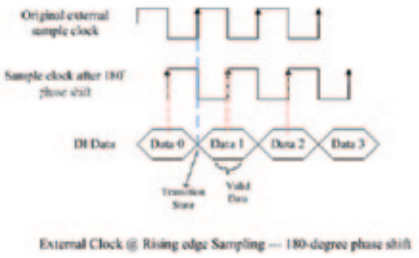
Initial power-up status for the onboard 32-channel I/O lines is as input lines. The 32-channel I/O lines are bi-directional and can be divided into four groups, each carrying 8 channels and individually configurable as an input or output port. The PCIe-7360 also supports software selectable logic levels of 1.8 V, 2.5 V, and 3.3 V, with all four groups matching the chosen logic level. In digital output mode, the outputs are tri-stated when the digital output lines are disabled. The programmable I/O direction and logic levels provide a flexible interface for devices under test (DUT).

Maximum Data Transfer Rate

The PCIe-7360 can support up to 400 MB/s throughput along with 32-bit data width at a maximum 100 MHz internal clock rate or 8/16-bit data width at a maximum 200 MHz external clock rate. The combination scatter-gather bus-mastering DMA, deep onboard 8 k-sample FIFO size, and x4 PCI Express® interface guarantee no data loss during sustained high-speed data processing.

Phase Delay

The PCIe-7360 features phase shifting of external sample clock or internal sample clock export, optimizing acquisition/generation timing in high-speed data transfer applications. The phase shifting of sample clock supports adjustment up to 80 steps, that is phase shifting from 4.5° to 355.5°, preventing erroneous sampling during transition states, such that sample timing is valid and stable.



I²C & SPI Serial Interfaces

PCIe-7360's application function I/O (AFI) can be configured as a I2C or SPI master node. The I2C interface supports fast mode and uses two bi-directional lines, SCL (serial clock) and SDA (serial data) respectively. The SPI interface uses four-wire signaling based on SCK (serial clock), SI (serial data input), SO (serial data output), and CS (chip select). Peripheral devices can communicate directly via the PCIe-7360's built-in I2C or SPI protocols along with provided APIs.

Features

- **x4 lane PCI Express® Interface**
- **8/16/24/32-CH at up to100MHz for DI or DO**
- **8/16-CH at up to 200MHz for DI in external clock mode**
- **400 MB/s maximum throughput**
- **Voltage level software selectable from 1.8 V, 2.5 V, and 3.3 V**
- **80-step phase shift in external clock mode**
- **Per group (8-bit) input/output direction selectable**
- **Support for I2C and SPI programmable serial interfaces for external device communication**
- **Scatter-gather DMA support**
- **Flexible handshake and external digital trigger modes**
- **8-channel auxiliary programmable I/O**

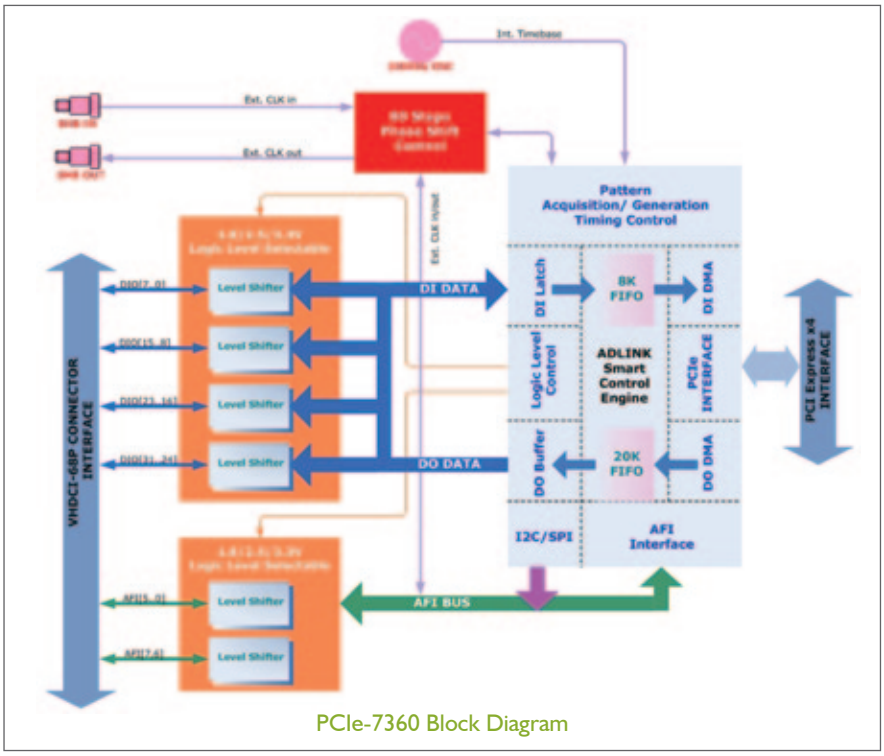
Software Support

OS Information

- Windows XP, Windows 7/8 x64/x86, Linux

Software Compatibility

- LabVIEW, MATLAB, Visual Studio.NET



PCIe-7360 Block Diagram

Specifications

Digital I/O

- 32-channels, per group (8-channel) input/output direction, with selectable logic levels: 1.8 V, 2.5 V, 3.3 V (software selectable)
- Power-up status: All digital inputs
- Impedance:
  - Input: 10 kΩ
  - Output: 50 Ω
- Input protection: -1 to 6 V
- Data transfer: Programmable I/O, bus-mastering DMA with scatter-gather
- Maximum data transfer rate: 400 MB/s
- Digital logic levels:

Logic Levels		1.8 V	2.5 V	3.3 V
Digital Input	Min. input high voltage	1.2 V	1.6 V	2 V
	Max. input low voltage	0.63 V	0.7 V	0.8 V
Digital Output	Min. output high voltage	1.6 V	2.3 V	3.1 V
	Max. output low voltage	0.2 V	0.2 V	0.2 V
	Max. output driving current	8 mA	16 mA	32 mA

Clocking Mode

- Internal clock: up to 100 MHz (100 MHz / N; 1<N<65535)
- External clock: up to 100 MHz (support 8/16/24/32-bit data width for DI/DO); up to 200 MHz (support 8/16-bit data width for DI only)
- Handshake
- Burst handshake

Trigger Sources

- Software trigger
- External digital trigger: AFI[0…7]

Trigger Modes

- Post trigger, Retrigger, Pattern match, Handshake

Change of State Interrupt

- Interrupt sources: Any of 32 channels or a pre-define channel change-of-state

Application Function I/O

- 8 channels
- Supported modes: static I/O, I²C or SPI master node, external clock input/output, external digital trigger input, handshake

Terminal Boards & Cables

- DIN-68H-01
  Terminal board with one 68-pin SCSI-VHDCI connector and 0 or 50 Ω jumper selectable impedance (Cables are not included.)
- ACL-10279
  - 68-pin SCSI-VHDCI cable with 50 Ω impedance
- SMB-SMB-1M
  - SMB to SMB cable, 1M

*** For more information about mating cables, please refer to P2-61/62.**

Ordering Information

PCIe-7360
100 MHz 32-CH High-Speed Digital I/O PCI Express® Card

ACL-10279

SMB-SMB-1M

DIN-68H-01

Pin Assignment

GND	68	34	GND
AFI7(DI CLK)	67	33	AFI6 (DO CLK)
GND	66	32	GND
D0	65	31	D1
AFI5	64	30	AFI4
D2	63	29	D3
GND	62	28	GND
D4	61	27	D5
AFI3	60	26	AFI2
D6	59	25	D7
GND	58	24	GND
D8	57	23	D9
GND	56	22	GND
D10	55	21	D11
GND	54	20	GND
D12	53	19	D13
AFI1	52	18	GND
D14	51	17	D15
GND	50	16	GND
D16	49	15	D17
GND	48	14	GND
D18	47	13	D19
GND	46	12	GND
D20	45	11	D21
GND	44	10	GND
D22	43	9	D23
GND	42	8	AFI0
D24	41	7	D25
GND	40	6	GND
D26	39	5	D27
GND	38	4	GND
D28	37	3	D29
GND	36	2	GND
D30	35	1	D31